Sub-threshold SRAM Sense Amplifier Compensation Using Auto-zeroing Circuitry

Peter Beshay, plb3qt@virginia.edu

Device variability in modern processes has become a major concern in SRAM design leading to degradation of both performance and yield. Variation induced offset in the sense amplifiers requires a larger bit-line differential, which slows down SRAM access times and causes increased power consumption. The effect aggravated in the sub-threshold region. In this paper, we propose a circuit that reduces the sense amp offset using an auto-zeroing scheme with automatic temperature, voltage, and aging tracking. The circuit enables flexible tuning of the offset voltage.

Offset Compensation, SRAM Sense Amplifier, and Auto-zeroing.

I. INTRODUCTION

Sub-threshold (sub-VT) design has proven useful for ultra-low-power and low-energy applications, like in the case of portable systems such as cellular phones and medical sensors. Dynamic energy consumption is reduced quadratically with VDD and minimum energy operation usually occurs in the sub-threshold region [1].

In sub-threshold circuits, the power supply is set below the transistor threshold voltage VT to obtain energy savings when speed is not the primary constraint. Sub-threshold circuits rely on leakage currents that are exponentially dependent on VT and are therefore more sensitive to process variations than traditional above-threshold designs [2]. This represents a primary challenge for designing sub-VT circuits. In addition, the sensitivity to process variations increases as CMOS devices continue shrinking.

Process variations cause input referred offset in the sense amplifiers (SAs), which require a larger bit-line differential. The effect is more dominant in particular in the sub-VT region because of the heightened variability effects on the drive current [3][7]. It is shown in [3] that the offset gets worse in sub-threshold relative to strong inversion as technology scales.

Worst case guard band SRAM design methodology accordingly increases the bit-line differential voltage ($\Delta V_{differential}$) during the Read operation to ensure robust output as shown in Figure 1 i.e. the magnitude of the voltage developed between BL0,$\overline{BL0}$ needs to be higher than the offset voltage of the sense amplifiers. This slows down SRAM access times and causes increased power consumption. The simple solution of upsizing the devices in the sense amplifier does not yield the reduction of input referred offset according to $1/(WL)^{0.5}$ that is achieved for strong inversion operation. Several attempts have been made before to tackle the problem of offset voltage in sense amplifiers including redundancy[4], transistor upsizing [5], digitally controlled compensation [6] and dynamic compensation[7]. Our approach to eliminating offset is a digital auto-zeroing (DAZ) scheme inspired by analog amplifier offset correction. The main advantages of the approach is the near-zero offset cancellation and the automatic temperature, voltage, and aging tracking through a repeated offset calibration phase, which makes the circuit in particularly useful for sub-threshold operation.

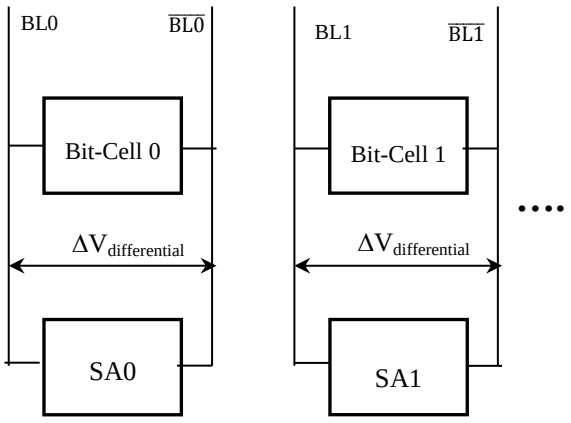


Figure 1. SRAM Read Path

II. MISMATCH COMPENSATION USING AUTO ZEROING CIRCUITRY

Auto-zeroing uses a split-phase clock and charge pump feedback circuit [8]. Figure 2 shows a latch-based sense amp with PMOS inputs. The same scheme can apply to a SA with NMOS inputs in an SRAM. Figure 3 shows the auto-zeroing circuit attached to the sense amp. The charge pump circuit is shown in Figure 4. ENI and ENO are the input voltage differential and offset tuning phases respectively. ER1 and ER2 are reset phases. During ER1, a zero differential input is applied to the sense amp. EN0 will then be applied, and the sense amp will resolve based on the intrinsic offset. The sense amp output is fed to the charge pump circuit that charges the capacitor Cp up or down. During ER2, the differential input is applied to the sense amp. ENI will then be applied, and the sense amp can resolve based on the differential input. Note that phases ENR1 and EN0 can be omitted or included based on how often re-calibration is needed. Transistors MC1 and MC2

control the drive strength of the right side of the sense amp to compensate for the offset.

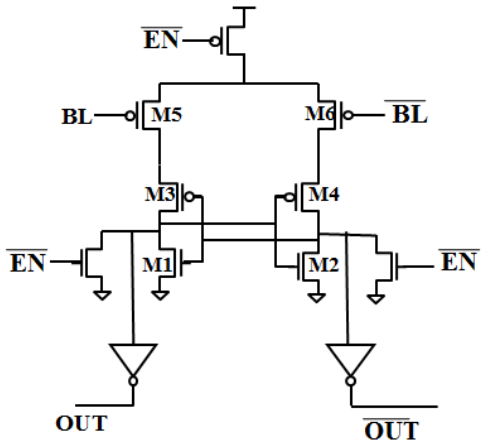


Figure 2. Latch-based sense amp

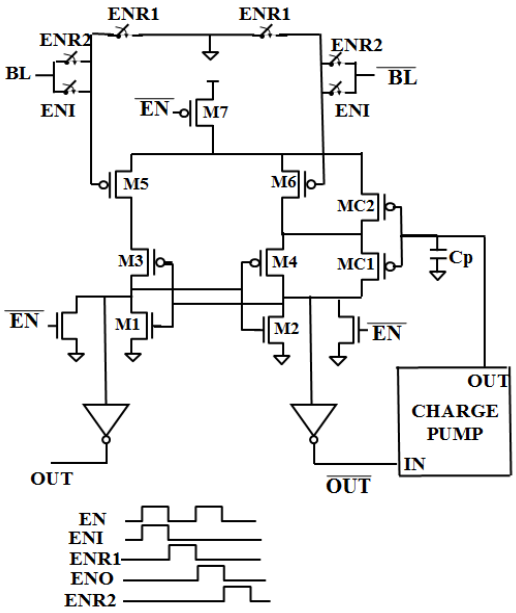


Figure 3. Auto-zeroing circuit attached to the sense amp

The charge pump controls the drive current in both transistors to equalize the strength of the sense amp right and left side to reduce the offset.

A supply voltage and clock frequency of 0.5 V and 1MHz are used in the simulations. The output voltage of the sense amp and the voltage on Cp are illustrated in Figure 5 for an input differential of − 10 mV. The initial voltage on Cp is zero. This causes an intrinsic positive offset voltage that set the SA output voltage to 1. Simulations indicate that the voltage on Cp required to auto-zero the offset is 142 mV. For a 10 mV offset, the voltage on Cp can vary within ±12 mV of the 142mV value.

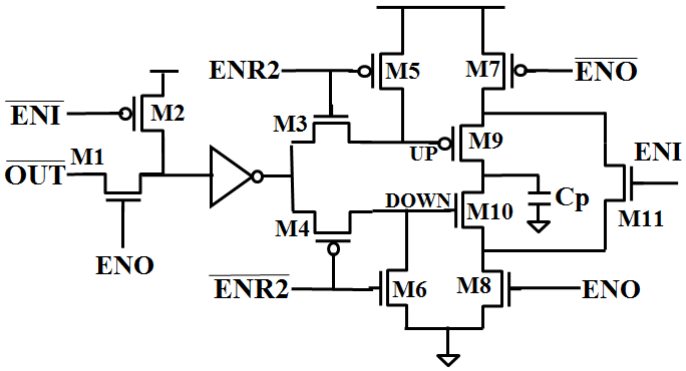


Figure 4. Charge Pump Circuit

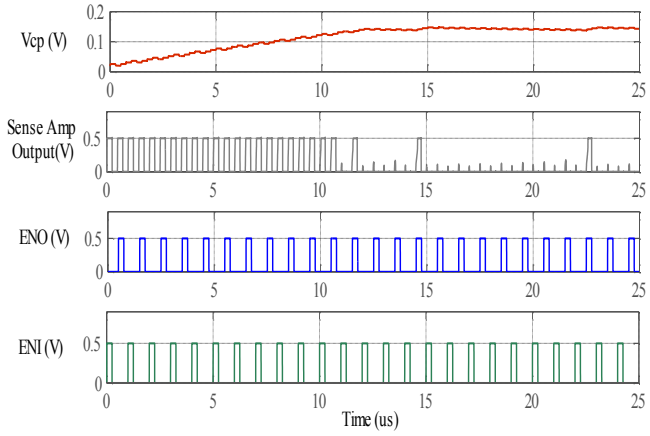


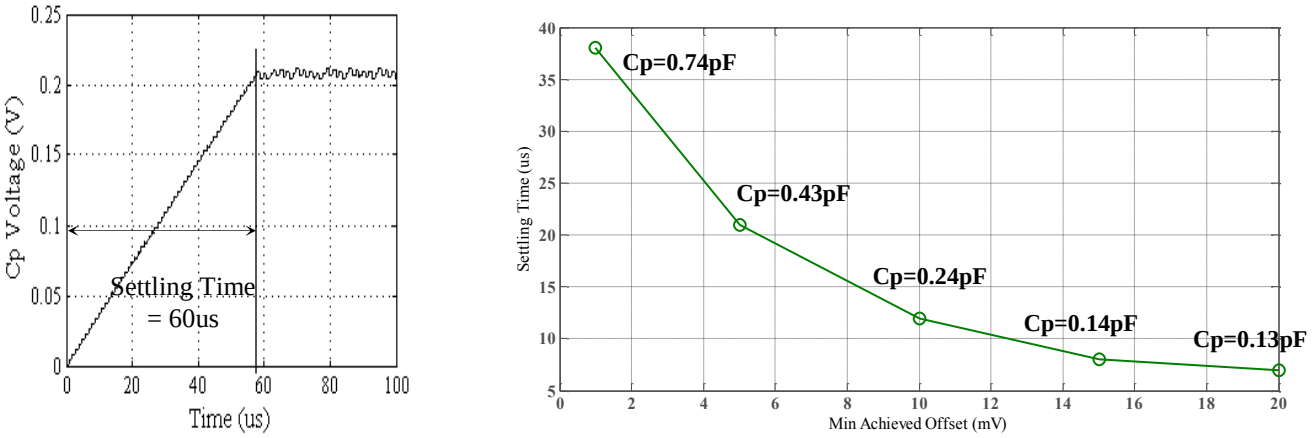
Figure 5. Charge Pump Circuit

III. VOLTAGE, TEMPERATURE, AND AGING TRACKING

To demonstrate temperature, voltage, and aging tracking, the offset voltage that remains after compensation is calculated for various voltages and temperatures. Results have shown that the circuit maintains the offset within 15mV for a 10% variations in the supply voltage [8], which can be considered as a marginal variation in the offset. The accuracy of voltage tracking depends on the supply voltage. Higher supply voltage causes more charges to be pumped to Cp during offset calibration phase, leading to coarser resolution. The results also demonstrate that the circuit maintains almost a constant offset across temperature [8]. To demonstrate aging tracking, we introduced an abrupt increase in Vth of MC2. The charge pump accordingly boosted the voltage on Cp to decrease the derive strength of MC2 to maintain the compensated offset voltage [8].

IV. OFFSET TUNING

The settling time is the difference between the time when the zero differential-input is applied and the time when the voltage of the output capacitor settles as shown in Figure 6a. Adjustment of the output capacitor (Cp) controls the quantity



(a) (b)

Figure 6. (a) Settling Time, (b) Min achieved offset vs. settling time for different values of output capacitor (Cp).

of charges added during the offset compensation phase (ENO) and so controls both the offset and the settling time. Figure 6b. demonstrates the trade-off between accuracy (min achieved offset) and settling time using different values of output capacitors. Accuracy can be tuned dynamically post-fabrication through tuning the frequency of external split phases making the circuit insensitive to the output capacitor variations.

V. 16KB SRAM DESIGN

A 20mV offset compensated DAZ SAs are used in a 16kB SRAM, in 45nm commercial technology node. The memory has one bank, 512 rows and 256 columns. The word size is 128bits. The energy and delay are compared to the uncompensated SAs case. The results show savings of 10% and 24% in the energy and delay respectively. Further analysis of the DAZ SAs with different structures (number of rows, banks, columns) of the 16kB SRAM indicate that structures with high number of rows benefits more from the scheme i.e. they have high improvement in both the energy and delay with the DAZ SAs.

VI. 45NM TEST CHIP MEASUREMENTS

A test chip fabricated in 45 nm technology is used to verify the scheme. The chip contains one regular SA array for benchmarking and another array that uses SAs with the auto-zeroing circuitry, with Cp equal to 32fF. The control signals are supplied to the auto-zeroing circuit at 1MHz. The measured mean (μ) and standard deviation (σ) of the uncompensated SA banks is − 31 mV and 45 mV respectively. The auto-zeroing circuitry reduced the value of μ to − 13mV and lowered σ to 9.3 mV. The scheme limits the absolute value of the maximum offset to 50 mV and improved σ of the offset by 80%.

VII. CONCLUSION

We proposed a circuit that is capable of reducing the sense-amp to near zero voltage inherently useful for sub-threshold region due to its ability to automatically track temperature, voltage and aging. Applying the scheme on a 16 kB SRAM in 45nm technology node showed a reduction in the total energy and delay of 10% and 15% respectively. Measurements from a test chip fabricated in 45 nm technology showed the circuit's ability to improve σ of the offset voltage by 80% and limited the absolute maximum value of the offset voltage to 50 mV using a 1 MHz split phase frequency and 32fF output capacitance.

VIII. REFERENCES

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